



(12) **United States Patent**
KHAMURA et al.
(10) Patent No.: **US 6,907,498 B2**
(45) Date of Patent: ***Jun. 14, 2005**

(54) **COMPUTER SYSTEM AND A METHOD OF ASSIGNING A STORAGE DEVICE TO A COMPUTER**

(75) Inventors: Masahito KHAMURA, Yokohama (JP); Kenji YAMAGAMI, Los Gatos, CA (US); Tetsuya MURAKAMI, Gifu-shi (JP)

(73) Assignee: Hitachi, Ltd., Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 269 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: 10/095,582

(22) Filed: Mar. 13, 2002

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US 2003/003182 A1 Jul. 11, 2003

Related U.S. Application Data

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(30) Foreign Application Priority Data
Aug. 27, 1999 (JP) 11-241,024

(31) Int. Cl. G06F 12/80

(52) U.S. Cl. 711/112; 711/152

(58) Field of Search 711/114, 152; 711/153, 156, 707/200; 709/222

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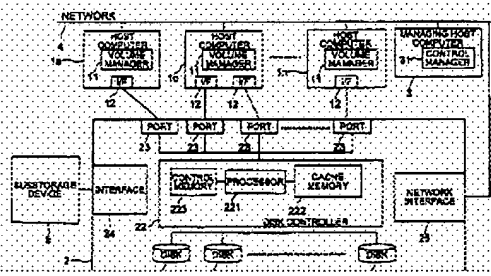
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Primary Examiner—KIMBER MORSEMAN
(74) Attorney, Agent, or Firm—Madingly, Stanger, Mahr, & Broadbridge, P.C.

(57) ABSTRACT

A computer system which has a plurality of computers and a storage device subsystem connected to the plurality of computers. The storage device subsystem has a plurality of storage devices and a plurality of interfaces, through which the subsystem is connected to the computers. One of the plurality of computers has a management means for holding therein data indicative of the storage devices and a connection relationship between the computers and storage device subsystem. Each computer, when wanting a new device, informs the management means of its capacity and type. The management means receives its notification and selects one of the storage devices which satisfies the request. And the management means instructs the storage device subsystem to set predetermined data in such a manner that the computer can access the selected device. The management means also returns predetermined data to the computer as a device assignment request, the assignment request computer modifies setting thereof to allow the computer in question can use the assigned device.

18 Claims, 33 Drawing Sheets



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(12) **United States Patent**
Yoshida et al.
(10) Patent No.: **US 6,883,064 B2**
(45) Date of Patent: **Apr. 19, 2005**

(34) **DISK ARRAY CONTROLLER COMPRISING A PLURALITY OF DISK ARRAY CONTROLLING UNITS**
(75) Inventors: Akira Yoshida, Hidao (JP), Shoji Nakamura, Odawara (JP)
(73) Assignee: Hitachi, Ltd., Tokyo (JP)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 101 days.
(21) Appl. No.: 10/076,456
(22) Filed: Feb. 19, 2002
(45) Prior Publication Data
US 2003/0084237 A1 May 1, 2003
(30) Foreign Application Priority Data
Oct. 30, 2001 (JP) 2001-33,858
(51) Int. Cl.⁷ G06F 13/00
(52) U.S. Cl. 711/114; 711/111; 711/112; 711/113
(56) Field of Search 711/111-114; 714/6
(30) References Cited

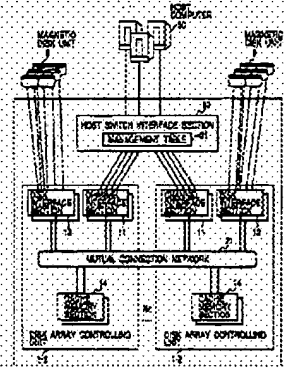
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Primary Examiner—Mano Padmanabhan
Assistant Examiner—John M. Ross
(74) Attorney, Agent, or Firm—Manning, Selvage & Main, P.C.

(37) **ABSTRACT**
"Disk array system is presented wherein the plurality of disk array controlling units operate as the sole disk array controller so as to maintain the performance of the cache memory sections of the respective disk array controlling units from deteriorating owing to their physical packaging locations and to maximize the performance thereof in proportion to the number of the controlling units in use. Disk array controller is provided, which controller comprises a host switch interface section, the plurality of respective disk array controlling units provided with a channel interface section, a disk interface section and a cache memory section and a mutual connection network in connection with the channel interface sections, the disk interface sections and the cache memory sections of the respective disk array controlling units. Access performance to the cache memory sections that are dispersively disposed between the respective disk array controlling units improves so as to enhance the performance of the disk array controller in proportion to the number of the disk array controlling units in use."

12 Claims, 8 Drawing Sheets



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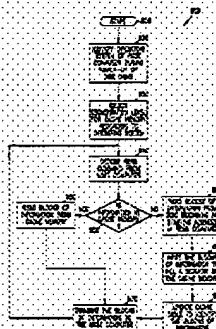
US006725330B1

(12) **United States Patent**
Wong et al.

(10) Patent No.: **US 6,725,330 B1**
(45) Date of Patent: **Apr. 20, 2004**

- (54) **ADAPTABLE CACHE FOR DISC DRIVE**
- (75) Inventors: Patrick Tai Hong Wong, Singapore (SG); Beng Woe Quak, Singapore (SG); YongPang Chng, Singapore (SG); Wesley Wing Hung Chan, Singapore (SG); WeiLoon Ng, Singapore (SG)
- (73) Assignee: Singate Technology LLC, Santa Valley, CA (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(d) by 683 days.
- (21) Appl. No.: 08/448,106
- (22) Filed: Aug. 25, 1999
- Related U.S. Application Data
- (60) Provisional application No. 60/131,201, filed on Aug. 27, 1999.
- (51) Int. Cl.⁷ G06F 12/00
- (52) U.S. Cl. 711/113; 711/129; 713/2
- (58) Field of Search 711/113, 129, 713/2, 1
- (56) References Cited
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- Primary Examiner—Matthew Kim
Assistant Examiner—Matthew D. Anderson
(74) Attorney, Agent, or Firm—David K. Liscinski; Derek J. Burger
- (57) **ABSTRACT**
- According to one embodiment of the present invention a disc controller in a disc drive includes a cache memory and a control circuit. The control circuit is configured to identify an operating system of a host computer coupled to the disc drive, select a segmentation level for the cache memory based on the identified operating system, and store information in the cache memory according to the segmentation level. According to another embodiment of the present invention a cache memory in a disc drive is operated by identifying an operating system of a host computer coupled to the disc drive, selecting a segmentation level for the cache memory based on the identified operating system, and storing information in the cache memory according to the segmentation level. The operating system is identified by reading a partition type from a master boot record stored in a disc in the disc drive.

17 Claims, 4 Drawing Sheets



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US06647461B2

(12) United States Patent
Fujimoto et al.
(10) Patent No.: US 6,647,461 B2
(45) Date of Patent: Nov. 11, 2003

- (54) DISK ARRAY CONTROLLER, ITS DISK
ARRAY CONTROL UNIT, AND INCREASE
METHOD OF THE UNIT
- (75) Inventors: Karahisa Fujimoto, Katsuhiko (JP);
Hiroaki Kamei, Higashiyama (JP);
Akira Fujibayashi, Kokubunji (JP);
Wataru Sekiguchi, Odawara (JP)
- (73) Assignee: Hitachi, Ltd., Tokyo (JP)
- (*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.
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- (21) Appl. No.: 10/335,899
(22) Filed: Jan. 3, 2003
(65) Prior Publication Data
US 2003/0103555 A1 Nov. 12, 2003
- JP 1996093 5/1999
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Related U.S. Application Data

- (60) Continuation of application No. 10/234,471, filed on Sep. 5,
2002, now Pat. No. 6,513,480, which is a continuation of
application No. 09/565,575, filed on Sep. 15, 2000, now Pat.
No. 6,477,619.
- Primary Examiner—Hiep T. Nguyen
(74) Attorney, Agent, or Firm—Anderson, Terry, Smith &
Kruza, LLP

Foreign Application Priority Data

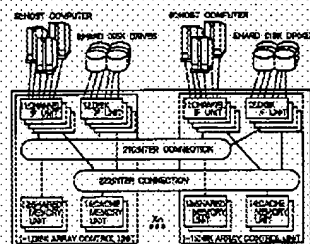
- Mar. 10, 2000 (JP) 2000-073669
(51) Int. Cl. G06F 12/02
(52) U.S. Cl. 711/114; 711/115; 711/146;
710/313; 710/316
(50) Field of Search 711/113, 114,
711/148; 710/31A, 31G

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5 Claims, 21 Drawing Sheets

ABSTRACT

A disk array controller is made up of multiple disk array
control units for implementing the data read/write operation
and each having channel IF units, disk IF units, cache
memory units and shared memory units. The disk array
controller further includes inter connections for intercon-
necting the shared memory units and interconnecting the
cache memory units across the border of disk array control
units. Theoretically alleviating the deterioration of performance
due to the data transfer between the disk array control units,
when the multiple disk array control units are to be operated
as a single disk array controller.



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